CLAIMS

Sub A1

1. A signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block, said signal processor comprising:

memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing;

error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block;

descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and

control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

2. A signal processor as described in Claim 1 wherein said error correction means comprises:

a syndrome calculator for calculating syndrome of the data which has been subjected to the predetermined digital signal

processing;

an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation;

error correction result holding means for holding information as to whether the data detected by the error position/pattern calculator is error-correctable or not;

data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and

number-of-error-correction control means for controlling the number of error corrections.

3. A signal processor as described in Claim 1 wherein said descrambling/error detection means comprises:

descrambling means for descrambling the data which has been corrected by the error correction means;

error detection means for detecting errors in the descrambled data; and

error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

4. A signal processor as described in Claim 1 wherein:

the data subjected to the predetermined digital signal processing is read from the memory means for each

predetermined error correction block, followed by error detection and error correction;

when there is some error, the error is corrected by the error correction means for each predetermined error correction block;

when there is no error, the data is transmitted to the display means for each predetermined error correction block.